**REMARKS**

This is in full and timely response to the Office Action mailed on June 2, 2004. Reexamination in light of the amendments and the following remarks is respectfully requested.

Claims 3 and 6-32 are currently pending in this application, with claims 3, 6 and 22 being independent. No new matter has been added.

**Specification objections**

The Office Action requests amendments to the Abstract.

While not conceding the propriety of this objection and in order to advance the prosecution of the above-identified application, the Abstract has been amended.

Regarding the use within the Abstract of the word "means", this word is used within the specification. A suggestion for alternative language would be greatly appreciated.

Regarding the alleged use within the Abstract of the word "said", this word is not found within the Abstract.

Regarding the alleged use within the Abstract of the phrase "such as", this phrase is not found within the Abstract. Instead, the phrase "in such a manner" is found within the Abstract.

Withdrawal of this objection is respectfully requested.

The Office Action objects to the term "the set information" found within the claims.

In response to this objection, term "the set information" is fully supported within the specification as originally filed. For example:

The specification as originally filed at page 9, lines 16-20, provides that "as the control means 110 controls the timings to generate both the timing signal and the address specifying signal in conformity with *the set information*, the test pattern cycle period for any address can be varied."

The specification as originally filed at page 9, lines 20-22, provides that "*the set information* is transferred to the semiconductor testing apparatus 100 prior to or during the test by some method."

The specification as originally filed at page 9, lines 23 to page 10, line 2, provides that "in execution of the test, the control means 110 always refers to the latest *set information* to thereby control the timings to generate the timing signal and the address specifying signal."

The specification as originally filed at page 11, lines 13-16, provides that "and *set information* for controlling the cycle period to execute the test pattern of each address is also set prior to start of the test."

The specification as originally filed at page 11, lines 17-22, provides that "upon start of the test, the control means 110 forms an operation reference signal to operate the test pattern, and generates a timing signal to produce a test pattern signal in conformity with *the set information*, and further generates an address specifying signal per cycle period for the test pattern memory means 130."

The specification as originally filed at page 12, lines 17-21, provides that "in this manner, as the control means 110 controls the timings to generate the timing signal and the address specifying signal in conformity with *the set information*, it becomes possible to freely set the test pattern cycle period of any desired address."

The specification as originally filed at page 13, lines 12-18, provides that "in this case, the cycle period rate of the entire test pattern is set to a value (RATE 1) lower than the maximum operation frequency and, in conformity with *the set information*,

the rate of the specific subject address only, i.e., the (N+3)-th cycle, is raised to a higher value (RATE 2)."

The specification as originally filed at page 13, line 24 to page 14, line 3, provides that "and the cycle frequency rate of the specific address can be successively narrowed by changing *the set information*, hence realizing confirmation of the maximum operation frequency in the relevant portion."

The specification as originally filed at page 19, line 19 to page 20, line 1, provides that "in the semiconductor testing apparatus of the present invention, as described hereinabove, a test pattern for a specified address is outputted at a timing corresponding to *set information*, in such a manner that the test pattern is supplied to the semiconductor device, which is being tested, at the timing that conforms with the predetermined *set information*, whereby a test pattern signal is generated on the basis of such test pattern."

The specification as originally filed at page 20, lines 1-4, provides that "as a result, the timing to generate the test pattern of the desired address is controlled in conformity with *the set information*, hence generating a desired test period."

Withdrawal of this objection is respectfully requested.

**Rejection under 35 U.S.C. §112, first paragraph**

Claims 1-5 were rejected under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the written description requirement. This rejection is traversed at least for the following reasons.

An adequate written description requirement ensures that the inventor had possession of the claimed subject matter at the time the application was filed. *In re Alton*, 37 USPQ2d 1578, 1584 (Fed. Cir. 1996).

"The purpose of the 'written description' requirement is broader than to merely explain how to 'make and use'; the applicant must also convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention." *Vas-Cath Inc. v. Mahurkar*, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991). See also M.P.E.P §2163.02.

"*How the specification accomplishes this is not material*. It is not necessary that the application describe the claim limitations exactly, but only so clearly that persons of ordinary skill in the art will recognize from the disclosure that the [Applicant] invented [the claimed invention] (emphasis added). *In re Wertheim*, 262, 191 USPQ 90, 96 (CCPA 1976). "The applicant does not have to utilize any particular form of disclosure to describe the subject matter claimed." *In re Alton*, 37 USPQ2d 1578, 1581 (Fed. Cir. 1996).

Claim 1 as originally filed

Originally filed claim 1 and the claims dependent thereon are drawn to a semiconductor testing apparatus wherein an input signal of a test pattern is supplied to a semiconductor device, and an output signal obtained from said semiconductor device is compared with a prescribed expected value to conduct a test, said apparatus comprising:

> test pattern memory means adapted for storing test pattern data of the test pattern, managing the test pattern data in accordance with addresses, and outputting the test pattern specified by any address;
>
> test pattern generation means for generating a test pattern signal on the basis of the test pattern outputted from said test pattern memory means; and
>
> control means for controlling said test pattern memory means and said test pattern generation means in such a manner that the test pattern signal based on the test pattern data of a desired address can be generated at a predetermined timing conforming to the set information.

Claim 4 as originally filed

Originally filed claim 4 and the claims dependent thereon are drawn to a semiconductor testing method for conducting a test of a semiconductor device by supplying an input signal of a test pattern to said semiconductor device and comparing an output signal therefrom with a prescribed expected value, said method comprising the steps of:

> managing and storing, in accordance with addresses, test pattern data of the test pattern generated previously;
>
> outputting the test pattern of a desired address at a predetermined timing that conforms with the set information; and
>
> generating a test pattern signal on the basis of the test pattern data of the desired address outputted at said predetermined timing.

But as noted hereinabove, the phrase "the set information" is fully supported within the specification as originally filed.

Withdrawal of this rejection is respectfully requested.

**Rejection under 35 U.S.C. §112, second paragraph**

Claims 1-5 were rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite. This rejection is traversed at least for the following reasons.

The Office Action contends that the term "the set information" found within claims 1 and 4 lacks an antecedent basis.

Regarding the rejection of originally filed claim 1, "the set information" is, itself, the first occurrence and need not require any additional antecedent basis. Usage of the definite article "the" is acceptable claim language in certain instances when presenting a first occurrence of a term. Note the recitation of "said set information" found within originally filed claim 2.

Regarding the rejection of claim 4, "the set information" is, itself, the first occurrence and need not require any additional antecedent basis. Usage of the definite article "the" is acceptable claim language in certain instances when presenting a first occurrence of a term. Withdrawal of this rejection is respectfully requested.

The Office Action contends that the term "the set information" found within originally filed claims 1 and 4 lacks an antecedent basis.

In response, the examples found within M.P.E.P. §2173.05(c) of claim language which have been held to be indefinite are fact specific and should not be applied as *per se* rules. In this regard, the language found within originally filed claims 1 and 4 of "in such a manner" has not been shown within M.P.E.P. §2173.05(c) to reach the definition of indefiniteness of 35 U.S.C. §112, second paragraph.

Withdrawal of this rejection is respectfully requested.

**New non-final Office Action**

If the allowance of claim 3 is not forthcoming at the very least and a new grounds of rejection made, then a ***new non-final Office Action*** is respectfully requested.

**Rejection under 35 U.S.C. §102**

Claims 1-5 were rejected under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 6,314,536 to Kurosaki.

This rejection is traversed at least for the following reasons.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Claim 3 has been placed into independent form and is drawn to a semiconductor testing apparatus wherein an input signal of a test pattern is supplied to a semiconductor device, and an output signal obtained from said semiconductor device is compared with a prescribed expected value to conduct a test, said apparatus comprising:

test pattern memory means adapted for storing test pattern data of the test pattern, managing the test pattern data in accordance with addresses, and outputting the test pattern specified by any address;

test pattern generation means for generating a test pattern signal on the basis of the test pattern outputted from said test pattern memory means; and

control means for controlling said test pattern memory means and said test pattern generation means in such a manner that the test pattern signal based on the test pattern data of a desired address can be generated at a predetermined timing conforming to the set information,

wherein said control means controls the timing of generation of the test pattern in such a manner that the cycle period rate to execute the test pattern of the desired address becomes a cycle period narrower than a predetermined rate.

Kurosaki arguably teaches a memory testing apparatus having pattern generator 2 that generates a test pattern signal S1 applied to a device to be tested MUT 3 (column 6, lines 14-18), and a system controller 6.

However, Kurosaki fails to disclose, teach or suggest the system controller 6 controlling the pattern generator 2 in such a manner that the cycle period rate to execute the test pattern S1 of the desired address becomes a cycle period narrower than a predetermined rate.

Thus, Kurosaki fails to disclose, teach or suggest a control means controls the timing of generation of the test pattern in such a manner that the cycle period rate to execute the test pattern of the desired address becomes a cycle period narrower than a predetermined rate.

Withdrawal of this rejection and allowance of the claims is respectfully requested.

**Newly added claims**

Claim 6 and the claims dependent thereon include the features of:

control means adapted to generate a timing signal and an address specifying signal, said timing signal having a test pattern cycle period, the duration of said test pattern cycle period being variable, the rate of modification for said address specifying signal being said test pattern cycle period;

test pattern memory means adapted to store a first test pattern, said first test pattern being outputted from said test pattern memory means in response to said address specifying signal, the rate of output for said first test pattern being said test pattern cycle period; and

test pattern generation means adapted to generate an input test pattern signal by combining said first test pattern with said timing signal, a semiconductor device under test receiving said input test pattern signal.

Claim 22 and the claims dependent thereon include the steps of:

generating a timing signal having a test pattern cycle period;

varying the duration of said test pattern cycle period;

generating an address specifying signal, the rate of modification for said address specifying signal being said test pattern cycle period;

storing a first test pattern within test pattern memory means;

outputting said first test pattern from within test pattern memory means in response to said address specifying signal, the rate of output for said first test pattern being said test pattern cycle period;

combining said first test pattern with said timing signal to generate an input test pattern signal, a semiconductor device under test receiving said input test pattern signal; and

comparing an output test pattern signal from said semiconductor device under test with said first test pattern.

These features are not found within Kurosaki, either expressly or implicitly. Allowance of the claims is respectfully requested.

**Conclusion**

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance. Accordingly, favorable reexamination and reconsideration of the application in light of the amendments and remarks is courteously solicited.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753. If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: September 2, 2004

Respectfully submitted,

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Attachments Abstract